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Sir:

Transmitted herewith for filing is the patent application of:

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For: **High-Speed, High Granularity Baud Clock Generation**

Enclosed are:

    8 sheets of drawings and 29 pages of Specification (including Abstract)
    __X__   Declaration/Power of Attorney
    __X__   Assignment with form PTO 1595

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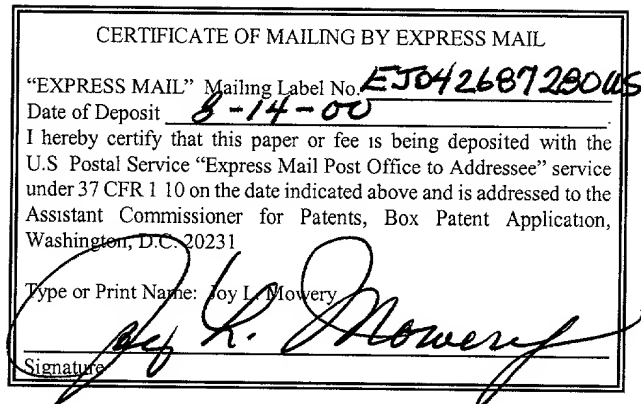
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HIGH-SPEED, HIGH GRANULARITY BAUD CLOCK GENERATION

FIELD OF THE INVENTION

The invention relates generally to baud clock generation and baud rate detection for serial communications and, more particularly, to baud clock generation and baud rate detection for serial communication interfaces that use oversampling and a fixed frequency clock.

BACKGROUND OF THE INVENTION

In conventional serial communication interfaces that use oversampling during data reception (also referred to herein as oversampling serial communication interfaces), for example universal asynchronous receiver/transmitters (UARTs), the baud rate is typically obtained by dividing the base clock rate of the interface by a number that is an integer

multiple of the oversampling factor. Thus, the possible baud rates are given by: base clock frequency/((oversampling factor) x (integer divisor)), where the oversampling factor is expressed, for example, in baud clock pulses (i.e., samples) per bit. If the base clock of the serial communication interface is set at a fixed frequency, as is typical, then there are

5   significant gaps between the possible baud rates. For example, for a base clock frequency of 1.8432 MHZ and an oversampling factor of 16 pulses/bit, the baud clock rates produced by using integer divisors of 1, 2 and 3 are 115,200 baud (bits/second in this example), 57,600 baud and 38,400 baud, respectively. Note the significant gap between the adjacent baud rates of 115,200 and 57,600. In this situation, if there is a need for a baud rate that does not fall

10   near any of the available baud rates, for example 76,800, it is typically necessary to provide a higher base clock frequency, from which an acceptable approximation of the desired baud rate can be derived. However, the increased base clock frequency disadvantageously requires an increase in the power used by the serial communication interface.

It is therefore desirable to increase the number of available baud rates without

15   increasing the base clock frequency of the serial communication interface.

The present invention provides for generation of a baud clock by dividing the base clock of the serial communication interface by one of a plurality of possible composite divisors. Each composite divisor is indicative of a minimum time interval between adjacent

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pulses of the associated baud clock, and further indicates that at least one pair of adjacent pulses within each symbol interval of the associated baud clock are to be separated by an extended time interval which is longer than the minimum time interval. The composite divisor advantageously results in a large number of available baud clock rates without increasing the base clock frequency.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 diagrammatically illustrates an exemplary embodiment of a baud clock generator according to the present invention.

FIGURE 2 diagrammatically illustrates an exemplary embodiment of the divisor generator of FIGURE 1.

FIGURE 3 diagrammatically illustrates an exemplary embodiment of the clock divider of FIGURE 1.

FIGURE 4 illustrates exemplary contents of the pulse pattern memory of FIGURE 3.

FIGURE 5 illustrates exemplary operations which can be performed by the clock divider embodiment of FIGURE 3.

FIGURE 6 is a timing diagram which illustrates an example of a baud clock signal generated by the clock divider of FIGURE 3.

FIGURE 7 diagrammatically illustrates another exemplary embodiment of the divisor generator of FIGURE 1.

FIGURE 8 illustrates a portion of the contents of an exemplary embodiment of the look-up table of FIGURE 7.

FIGURE 9 diagrammatically illustrates pertinent portions of an exemplary embodiment of a data processing and communication system according to the invention.

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FIGURE 10 illustrates exemplary operations which can be performed by the embodiments of FIGURES 1-9.

FIGURE 11 illustrates an exemplary embodiment of a baud rate detector according to the invention.

DETAILED DESCRIPTION

FIGURE 1 diagrammatically illustrates an exemplary embodiment of a baud clock

generator according to the invention. The baud clock generator can be provided, for

example, in an oversampling serial communication interface such as a UART. In FIGURE 1,

information indicative of the desired baud rate, for example in units of bits/second, is input

to a divisor generator 11. In response to the desired baud rate, the divisor generator 11

produces and outputs an enhanced granularity divisor D_{EG}. This enhanced granularity divisor

is a composite divisor including a first divisor component D and a second divisor component

REMD. These divisor components are input to a clock divider 13 which, in response to the

first and second divisor components, divides the base clock signal of the oversampling serial

communication interface to produce a baud clock signal that approximates the desired baud

rate. The baud clock signal 15 is provided to a sampler of the oversampling serial

communication interface, which can use the baud clock signal in conventional fashion to

sample serial communication data received at the interface. The baud clock signal 15 can

also be used in conventional fashion to transmit data from the interface.

The first divisor component D corresponds to the aforementioned integer divisor that

is conventionally used to generate baud rates. Using the conventional technique, the integer

divisor that will produce the closest approximation to a desired baud rate is given by the

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quotient of the following division operation: base clock frequency/(K x desired baud rate), where K is the oversampling factor associated with the oversampling serial communication interface. Advantageously, the invention utilizes also the modulo K remainder produced by this division operation. By using the modulo K remainder, the invention produces K-1 intermediate baud rates between any given pair of adjacent baud rates that would be produced by the conventional technique. The second divisor component REMD of FIGURE 1 corresponds to this modulo K remainder.

FIGURE 2 diagrammatically illustrates an exemplary embodiment of the divisor generator of FIGURE 1. In the embodiment of FIGURE 2, a multiplier 31 multiplies the desired baud rate by the oversampling factor K. A divider 35 divides the base clock rate of the serial communication interface by the output 33 of the multiplier 31, namely K x (desired baud rate), producing a quotient and a modulo K remainder. The modulo K remainder is the second divisor component REMD of FIGURE 1, and the quotient is the first divisor component D of FIGURE 1.

FIGURE 3 diagrammatically illustrates an exemplary embodiment of the clock divider 13 of FIGURE 1. In this embodiment, the base clock of the serial communication interface is applied to the count input of a base clock counter 51 which counts pulses of the base clock. After a predetermined number of base clock pulses, the output 58 of counter 51

triggers a pulse generator 52 to output a baud clock pulse. The counter 51 includes a load

select input 52 that determines which of two possible target count values will be loaded into

the counter 51. More specifically, the counter 51 is selectively loaded with a target count

value of D or D + 1 in response to input 52. Thus, when D is selected as the target count

5 value, the counter 51 triggers a baud clock pulse for every D pulses of the base clock.

Similarly, when D + 1 is selected as the target count value, the counter 51 triggers a baud

clock pulse for every D + 1 pulses of the base clock.

The load select input 52 is driven from a pulse pattern memory 54 that includes K

entries, one for each possible value of the modulo K remainder REMD. Each of the K

10 entries in the pulse pattern memory 54 includes K bits having a value of either 1 or 0. The

second divisor component REMD is input to the pulse pattern memory 54, and selects the

corresponding one of the K entries. The pulse pattern memory 54 has a pointer input 56

which points to one of the K bits of the entry selected by REMD. The pointer value at 56 is

provided by a baud clock counter 53 whose count input is coupled to the baud clock 15. The

15 counter 53 counts cyclically through K states, thereby repeatedly tracking the K baud clock

pulses used to sample each bit received at the serial communication interface. The output

count value of counter 53 is provided as the pointer value at 56. Thus, for each baud clock

pulse within a given bit interval of the serial communication interface, the pointer 56 points

to a specific one of the K bit locations in the pulse pattern memory entry selected by REMD. If the bit value pointed to is 0, then the pulse pattern memory 54 outputs a load select value of 0, thereby selecting D to be loaded as the count target for counter 51. If the bit value pointed to is 1, then the pulse pattern memory 54 outputs a load select value of 1, thereby selecting D + 1 to be loaded as the count target for counter 51.

FIGURE 4 illustrates exemplary contents of the pulse pattern memory 54 of FIGURE 3. In this example, the oversampling factor K is 16, so there are 16 entries in the pulse position memory, each entry having 16 bits. For this oversampling factor of K=16, and recalling that REMD is a modulo K remainder, there are 16 possible values of REMD, namely 0-15. As shown in FIGURE 4, the entry corresponding to REMD=0 includes all 0s. In this instance, all pulses of the baud clock will be separated from one another by a time interval corresponding to D pulses of the base clock, just as in the prior art.

As shown by the example of FIGURES 3 and 4, a non-zero value of REMD specifies a number of pairs of adjacent pulses within each bit interval of the baud clock 15 will be separated by a time interval corresponding to D+1 pulses of the base clock. That is, for example, when REMD=1, the corresponding entry in the pulse position memory has one bit with a value of 1, so there will be a time interval corresponding to D+1 base clock pulses between 1 pair of adjacent pulses in each bit interval of the baud clock. This time interval

corresponding to D+1 base clock pulses is longer than the aforementioned time interval

associated with D base clock pulses and, in this example, will occur between the third and

fourth baud clock pulses of each bit interval, because the fourth bit in the pulse pattern

memory entry corresponding to REMD=1 has a value of 1. Similarly, for a value of

5　REMD=2, two pairs of adjacent baud clock pulses in each bit interval will be separated by

the longer (D+1) time interval, namely the third and fourth pulses and the eleventh and

twelfth pulses. As can be seen in the example of FIGURE 4, it can be advantageous to

distribute the 1s approximately evenly within the respective pulse position memory entries,

thus approximately evenly distributing the longer time intervals throughout the bit interval.

FIGURE 5 illustrates exemplary operations which can be performed by the clock

divisor of embodiment of FIGURE 3. After initializing base clock and baud clock count

values at 80 and 81, respectively, the first base clock pulse is received at 82, causing the base

clock count to increment by one. It is thereafter determined at 83 whether the pulse pattern

memory bit selected by REMD and the baud clock count value is 1 or 0. If the selected bit

15　is 0, then D base clock pulses will be counted, as illustrated at 84. If the selected bit is 1,

then D + 1 base clock pulses will be counted, as illustrated at 85. After the selected number

(D or D+1) of base clock pulses have been counted at 84 or 85, a baud clock pulse is

generated at 86. The baud clock pulse at 86 causes the baud clock count value to increment

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by one as shown at 87. The aforementioned steps at 81-87 are then repeated until the end of the current bit interval is reached at 88, namely when the baud clock count value reaches K. At this point, the count values are reset again at 80 and 81.

FIGURE 6 is a timing diagram which illustrates an example of the baud clock 15 produced by the clock divider embodiment of FIGURE 3. In the example of FIGURE 6, the oversampling factor K is 16 and REMD=8. The value of D sets the minimum time interval (D base clock cycles) between the leading edges of any two adjacent baud clock pulses, and the value of D+1 defines an extended time interval (D+1 base clock cycles) between selected pairs of adjacent baud clock pulses. In the FIGURE 6 example, the alternating sequence of minimum time intervals associated with count value D and extended time intervals associated with count value D + 1 conforms to the alternating sequence of 0s and 1s in the FIGURE 4 pulse position memory entry corresponding to REMD=8. In the example of FIGURE 6, the overall length of each bit interval is 8xD+8(D+1)=16D+8 base clock cycles. If D=3, for example, the bit interval length is 56 base clock cycles. This corresponds exactly to the baud rate given by: base clock rate/(K x D + REMD), for K=16, D=3 and REMD=8 which is: base clock rate/56. Although the example of FIGURE 6 shows 16 baud clock pulses per bit interval, it will be clear to workers in the art that the invention is more generally applicable to any baud clock having K pulses per symbol interval.

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Returning now to the aforementioned example of a desired baud rate of 76,800, an

oversampling factor of K=16 and a base clock rate of 1.8432 MHZ, the embodiment of

FIGURE 2 yields D=1 and REMD=8. These values of D and REMD will yield a baud rate

of: $1.8432 \times 10^6/16(1) + 8 = 76,800$. As another example, for a desired baud rate of 82,000,

5   an oversampling factor of K=16 and a base clock rate of 1.8432 MHZ, the embodiment of

FIGURE 2 yields D=1 and REMD=6. Thus, the resultant baud rate will be:

$1.8432 \times 10^6/16(1) + 6 = 83,781.8$. This baud rate approximates the desired 82,000 rate

significantly more closely than do the two closest possibilities yielded by the aforementioned

prior art technique, namely 115,200 or 57,600.

10   FIGURE 7 illustrates another exemplary embodiment of the divisor generator of

FIGURE 1. The embodiment of FIGURE 7 utilizes a look-up table 43 to produce the first

and second divisor components D and REMD. As illustrated in more detail in FIGURE 8,

the look-up table at 43 can index the possible pairs of values of D and REMD against

respective baud rate ranges. For a given oversampling factor of K, there are K possible

15   values of REMD (0 through K-1) for each possible value of D, because REMD is a modulo

K remainder. Again using the example of a 1.8432 MHZ base clock rate and an

oversampling factor of K=16: if D=1 and REMD=0, then the baud rate is 115,200; if D=1

and REMD=1, then the baud rate will be 108,423.5; and if D=1 and REMD=2, then the baud

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rate will be 102,400. Thus, for example, Range 2 in the look-up table of FIGURE 8 could extend from a value halfway between 115,200 and 108,423.5 to a value halfway between 108,423.5 and 102,400. If the desired baud rate falls within Range 2, then the baud rate provided by the baud clock of FIGURE 1 will be 108,423.5, namely the baud rate associated

5   with D=1 and REMD=1. The embodiment of FIGURE 7 includes a range classifier 41 which receives the desired baud rate and determines which of the ranges, Range 1, Range 2, etc. contains the desired baud rate. The range determined by the range classifier 41 is then input to the look-table 43, and corresponding values of the first and second divisor components D and REMD are output from the look-table.

10   It can be seen from FIGURES 1-8 that the composite nature of the enhanced granularity divisor D_{EG} advantageously results in K-1 intermediate baud rates available between each pair of adjacent baud rates produced using the conventional technique. For example, with a base clock frequency of 1.8432 MHZ and an oversampling factor of K=16, there are 15 intermediate baud rates (corresponding to REMD=1-15) available between

15   115,200 (D=1 and REMD=0) and 57,600 (D=2 and REMD=0).

FIGURE 9 diagrammatically illustrates pertinent portions of an exemplary data processing and communication system according to the present invention. In FIGURE 9, a data processing apparatus 61 is coupled at 69 for serial communication with one or more

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external devices shown generally at 63. The data processing apparatus 61 includes data

processing circuitry 65 and a serial communication interface 67 coupled to the data

processing circuitry 65 for permitting serial communication between the data processing

circuitry 65 and the external device(s) 63. In the exemplary embodiment illustrated in

5   FIGURE 9, the serial communication interface 67 is a UART including the baud clock

generator of FIGURE 1. The data processing circuitry 65 can perform any desired data

processing operation(s) on data communicated between the data processing apparatus 61 and

the external device(s) 63.

In one example, the data processing apparatus 61 is a microprocessor or digital signal

10   processor, and the external device(s) at 63 can be any external device with which

microprocessors and digital signal processors can communicate via the serial communication

path shown diagrammatically at 69. For example, the external device(s) at 63 could be some

other microprocessor(s) or digital signal processor(s). In some exemplary embodiments, the

serial communication path at 69 is an RS-232 link.

15   In another example, the data processing apparatus 61 is the central processing unit

(CPU) of a desktop or laptop computer, and the external device(s) at 63 is a keyboard,

mouse, printer or any device that provides a man-machine interface to the central processing

unit. In a further example, the data processing apparatus 61 and the external device(s) at 63

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are modems coupled via serial interface(s) to permit communication between further devices that are not explicitly shown in FIGURE 9. In a still further example, the data processing apparatus 61 is a radiotelephone and the external device 63 is a laptop or desktop computer.

FIGURE 10 illustrates exemplary operations which can be performed by the embodiments of FIGURES 1-9. It is first determined at 71 whether a new baud rate is desired. If so, then D and REMD are obtained at 73. Thereafter D and REMD are used at 75 to produce the baud clock from the base clock.

FIGURE 11 diagrammatically illustrates an example of a baud rate detector with which an external device such as shown at 63 in FIGURE 9 can determine what baud rate is being used by the communication interface 67 of FIGURE 9. In the example of FIGURE 11, a counter counts the number of base clock cycles that occur during the START bit conventionally associated with the incoming data. Assuming in this example an oversampling factor K = 16, the 4 (2^4 = 16) least significant bits of the output count value will represent REMD (REMD = 1 in this example) and the remaining most significant bits represent D (D = 1 in this example). These D and REMD values can then be applied to the clock divider 13 of FIGURES 1 and 3, which can then produce the baud clock needed to sample the incoming data. Thus, the baud rate detector of FIGURE 11 is another example of a divisor generator for use with the clock divider 13.

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It should be evident from the foregoing that use of the enhanced granularity divisor including first and second divisor components according to the present inventions provides a significantly larger number of available baud rates given a fixed base clock frequency. This permits the desired baud rate to be approximated much more closely than in the prior art, particularly at relatively high baud rates. This closer approximation can advantageously be provided without requiring an increase in the base clock frequency.

Although exemplary embodiments of the invention are described above in detail, this does not limit the scope of the invention, which can be practiced in a variety of embodiments.

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WHAT IS CLAIMED IS:

1.　A method of generating from a base clock signal having a predetermined frequency a baud clock signal for use in serial communications, comprising:

selecting a desired baud rate;

in response to the desired baud rate, providing a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

dividing the base clock signal in response to said composite divisor to produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

2.　The method of Claim 1, including providing an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock signal, said step of providing a composite divisor including providing the composite divisor in response to the oversampling factor and the desired baud rate.

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3.   The method of Claim 1, wherein the composite divisor includes a first divisor component indicative of the minimum time interval and a second divisor component which indicates that the leading edges of at least one pair of adjacent pulses are to be separated by the extended time interval.

5   4.   The method of Claim 3, wherein said step of providing a composite divisor includes dividing the predetermined frequency of the base clock signal by the desired baud rate and by the oversampling factor to produce a quotient and a remainder, providing the quotient as the first divisor component, and providing the remainder as the second divisor component.

10   5.   The method of Claim 4, wherein the remainder is modulo K, and K is the oversampling factor.

6.   The method of Claim 3, wherein said step of providing a composite divisor includes providing a plurality of possible values of the first divisor component and providing for each of the possible values of the first divisor component a plurality of possible values

15   of the second divisor component.

7.   The method of Claim 6, including providing an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock

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signal, and producing the possible values of the second divisor component based on the oversampling factor.

8.   The method of Claim 3, wherein said step of providing a composite divisor includes selecting from among a plurality of pairs of first and second divisor components one pair that will produce in said dividing step a baud clock signal having a baud rate that more closely approximates the desired baud rate than any other baud clock signal that could be produced in said dividing step using any of the remaining pairs of first and second divisor components.

9.   The method of Claim 8, wherein said step of providing a composite divisor includes indexing the plurality of pairs of first and second divisor components against respective baud ranges.

10.   The method of Claim 3, wherein said dividing step includes determining the minimum time interval and the extended time interval in response to the first divisor component and the predetermined frequency of the base clock signal, and selecting the at least one pair of adjacent pulses in response to the second divisor component.

11.   The method of Claim 10, wherein said selecting step includes selecting in response to the second divisor component a plurality of pairs of adjacent pulses within each

symbol interval of the baud clock signal whose respective pairs of leading edges are to be separated by the extended time interval.

12.   An apparatus for generating a baud clock signal for use in a serial communication interface, comprising:

a first input for receiving a base clock signal having a predetermined frequency;

a second input for receiving information indicative of a desired baud rate;

a divisor generator coupled to said second input for providing in response to the desired baud rate a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

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13.   The apparatus of Claim 12, wherein the composite divisor includes a first divisor component indicative of the minimum time interval and a second divisor component which indicates that the leading edges of at least one pair of adjacent pulses are to be separated by the extended time interval.

14.   The apparatus of Claim 13, wherein said divisor generator includes a divider for dividing the predetermined frequency of the base clock signal by the desired baud rate and by an oversampling factor indicative of a number of baud clock pulses within each symbol interval of the baud clock signal to produce a quotient and a remainder, and wherein the quotient is the first divisor component and the remainder is the second divisor component.

15.   The apparatus of Claim 14, wherein the remainder is a modulo K remainder, and wherein K is the oversampling factor.

16.   The apparatus of Claim 13, wherein said divisor generator includes a look-up table having stored therein information indicative of a corresponding relationship between a plurality of baud rate ranges and respective pairs of said first and second divisor components.

17.   The apparatus of Claim 13, wherein said clock divider includes a base clock counter responsive to said base clock and said first divisor component for determining said

minimum time interval and said extended time interval, a pulse generator coupled to said

base clock counter for producing the baud clock signal in response to operation of said base

clock counter, and a pulse position memory coupled to said base clock counter for storing

information indicative of the at least one pair of adjacent pulses that are to be separated by

5   the extended time interval.

18.   The apparatus of Claim 17, wherein said pulse position memory includes an

input for receiving said second divisor component, said pulse position memory responsive

to said second divisor component for selecting said information indicative of the at least one

pair of adjacent pulses.

10   19.   The apparatus of Claim 18, wherein said pulse position memory includes a

plurality of entries and is responsive to said second divisor component for selecting one of

said entries, said clock divider including a baud clock counter coupled to said pulse generator

for counting pulses of said baud clock signal, said baud clock counter having an output

coupled to said pulse position memory, said pulse position memory responsive to said output

15   of said baud clock counter for selecting a portion of said one entry.

20.   The apparatus of Claim 12, wherein the serial communication interface is a

UART.

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21.   A data processing apparatus capable of serial communication with an external

device, comprising:

data processing circuitry for performing data processing operations on data involved

in serial communication with the external device;

5   a serial communication interface coupled to said data processing circuitry for

permitting serial communication between said data processing circuitry and the external

device; and

a baud clock generator for generating a baud clock signal for use by the serial

communication interface, said baud clock generator including a first input for receiving a

10   base clock of the serial communication interface, said base clock having a predetermined

frequency, a second input for receiving information indicative of a desired baud rate, a

divisor generator coupled to said second input for providing in response to the desired baud

rate a composite divisor which is indicative of a minimum time interval by which leading

edges of adjacent pulses of the baud clock signal are to be separated and which further

15   indicates that leading edges of at least one pair of adjacent pulses within each symbol interval

of the baud clock signal are to be separated by an extended time interval which is longer than

said minimum time interval, and a clock divider coupled to said first input and said divisor

generator and responsive to said composite divisor for dividing said base clock signal to

produce a baud clock signal which has a baud rate that approximates the desired baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

5   22.   The apparatus of Claim 21, wherein said serial communication interface is a UART.

23.   The apparatus of Claim 21, provided as one of a microprocessor, a digital signal processor, a modem, and a radiotelephone.

24.   A data processing communication system, comprising:

a data processing apparatus and a device coupled externally to the data processing apparatus via a serial communication path;

said data processing apparatus including data processing circuitry for performing data processing operations on data involved in serial communication with said externally coupled device, a serial communication interface coupled between said data processing circuitry and said serial communication path for permitting serial communication between said data processing circuitry and the externally coupled device, and a baud clock generator for generating a baud clock signal for use by the serial communication interface; and

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said baud clock generator including a first input for receiving a base clock of the

serial communication interface, said base clock signal having a predetermined frequency, a

second input for receiving information indicative of desired baud rate, a divisor generator

coupled to said second input for providing in response to the desired baud rate a composite

5   divisor which is indicative of a minimum time interval by which leading edges of adjacent

pulses of the baud clock signal are to be separated and which further indicates that leading

edges of at least one pair of adjacent pulses within each symbol interval of the baud clock

signal are to be separated by an extended time interval which is longer than said minimum

time interval, and a clock divider coupled to said first input and said divisor generator and

10   responsive to said composite divisor for dividing said base clock signal to produce a baud

clock signal which has a baud rate that approximates the desired baud rate and which has

within each symbol interval thereof at least said minimum time interval between the leading

edges of all adjacent pulses thereof and said extended time interval between the leading

edges of at least one pair of adjacent pulses thereof.

15   25.   The system of Claim 24, wherein said data processing apparatus is one of a

microprocessor, a digital signal processor, a modem, a radiotelephone and a central

processing unit of a laptop or desktop computer.

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26.   The system of Claim 25, wherein the externally coupled device is one of a

microprocessor, a digital signal processor, a modem, a keyboard, a mouse, a printer and a

laptop or desktop computer.

27.   The system of Claim 24, wherein the externally coupled device is one of a

5   microprocessor, a digital signal processor, a modem, a keyboard, a mouse, a printer and a

laptop or desktop computer.

28.   A method of generating from a base clock signal having a predetermined

frequency a baud clock signal for use in receiving incoming data in serial communications,

comprising:

receiving the incoming data at an unknown baud rate;

in response to the incoming data, providing a composite divisor which is indicative

of a minimum time interval by which leading edges of adjacent pulses of the baud clock

signal are to be separated and which further indicates that leading edges of at least one pair

of adjacent pulses within each symbol interval of the baud clock signal are to be separated

15   by an extended time interval which is longer than said minimum time interval; and

dividing the base clock signal in response to said composite divisor to produce a baud

clock signal which has the unknown baud rate and which has within each symbol interval

thereof at least the minimum time interval between the leading edges of all adjacent pulses

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thereof and the extended time interval between the leading edges of at least one pair of adjacent pulses thereof.

29. The method of Claim 28, wherein said providing step includes providing the composite divisor in response to a start bit of the incoming data.

5   30. An apparatus for generating a baud clock signal for use in receiving incoming data in a serial communication interface, comprising:

a first input for receiving a base clock signal having a predetermined frequency;

a second input for receiving the incoming data at an unknown baud rate;

a divisor generator coupled to said second input for providing in response to the

10   incoming data a composite divisor which is indicative of a minimum time interval by which leading edges of adjacent pulses of the baud clock signal are to be separated and which further indicates that leading edges of at least one pair of adjacent pulses within each symbol interval of the baud clock signal are to be separated by an extended time interval which is longer than said minimum time interval; and

15   a clock divider coupled to said first input and said divisor generator and responsive to said composite divisor for dividing said base clock signal to produce a baud clock signal which has the unknown baud rate and which has within each symbol interval thereof at least the minimum time interval between the leading edges of all adjacent pulses thereof and the

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extended time interval between the leading edges of at least one pair of adjacent pulses

thereof.

ABSTRACT

A baud clock (15) for use by a serial communication interface (67) is generated by

dividing a base clock of the serial communication interface by one of a plurality of possible

composite divisors (D_{EG}). Each composite divisor is indicative of a minimum time interval

by which adjacent pulses of the baud clock are to be separated, and further indicates that at

least one pair of adjacent pulses within each symbol interval of the baud clock are to be

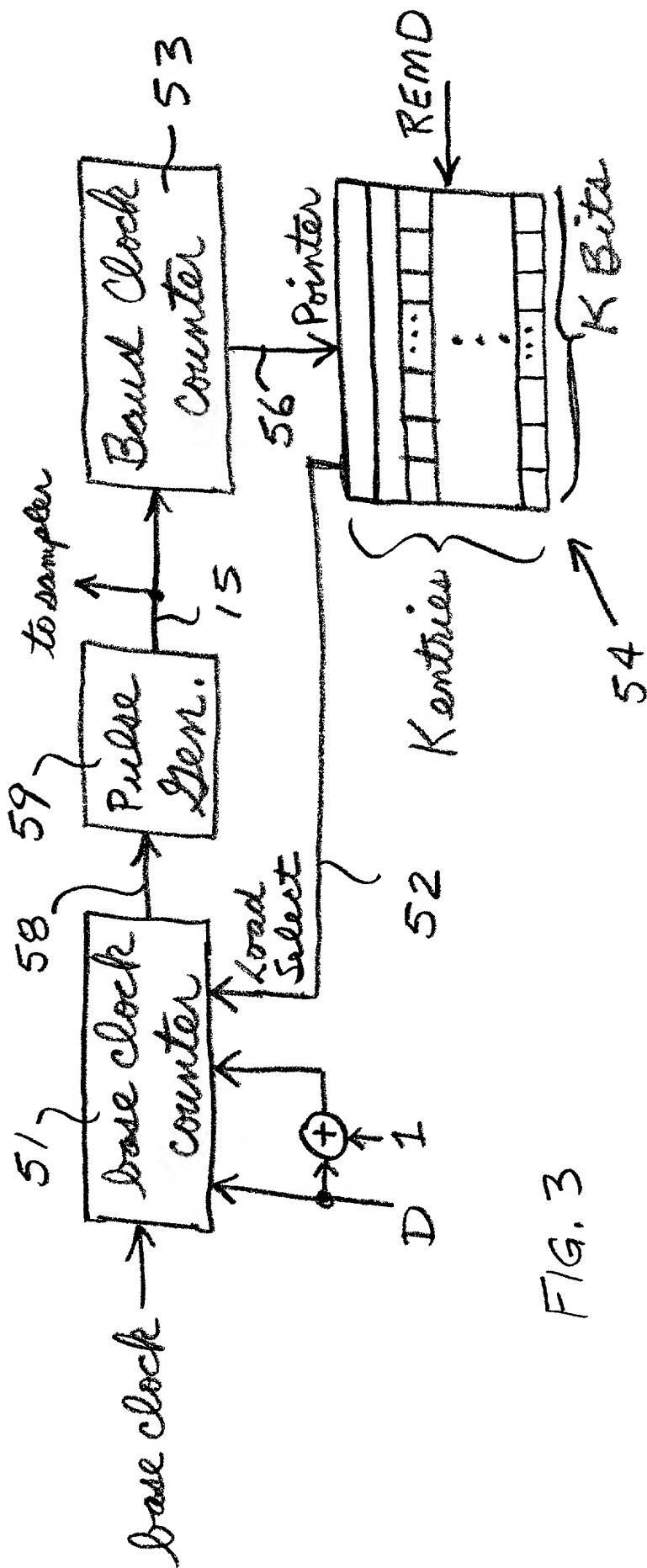separated by an extended time interval which is longer than the minimum time interval.
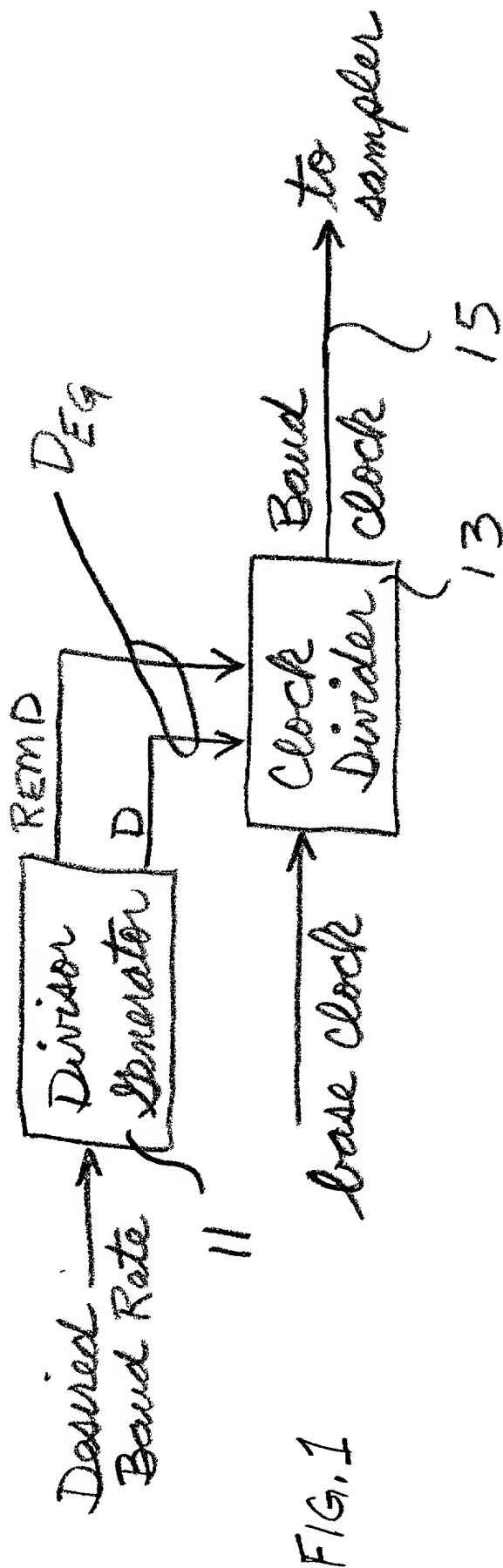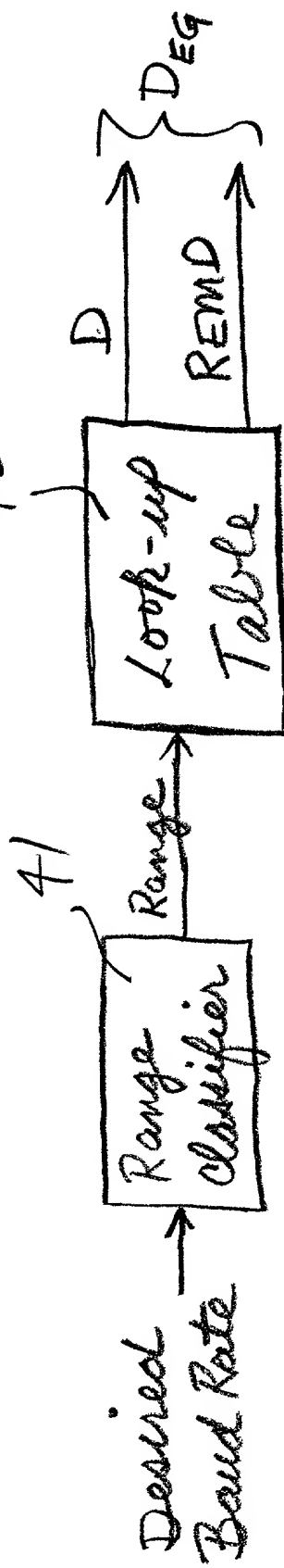
102521.000028: 2427169.1

FIG. 1

Desired Baud Rate → Divisor Generator (11)

REMD, D_{Eq}, D → Clock Divider (13)

Base Clock → Clock Divider

Baud Clock → to sampler (15)

FIG. 3

Base Clock → Base Clock Counter (51)

D, 1 → (+) → Load Select (52)

Base Clock Counter (51) → Pulse Gen. (59) (58) → to sampler (15)

Baud Clock Counter (53)

Pointer (56)

REMD

K entries, K Bits (54)

FIG. 2

Base clock rate → 35 [÷] → D (quotient)

Desired Baud Rate → 33 → [X] 31 ← K (oversampling factor)

→ REMD (Mod K remainder) $\left\}D_{EG}\right.$

001.0100 101100 001.00

FIG. 7

Desired Baud Rate → [Range Classifier] 41 → Range → [Look-up Table] 43 → D

→ REMD $\left\}D_{EG}\right.$

REMD

0 →	0000000000000000
1 →	0001000000000000
2 →	0001000000010000
3 →	0101000000010000
4 →	0101000000010100
5 →	0101010000010100
6 →	0101010000010101
7 →	0101010100010101
8 →	0101010101010101
9 →	0101011101010101
10 →	0101011101010111
11 →	0111011101010111
12 →	0111011101110111
13 →	0111111101110111
14 →	0111111111110111
15 →	1111111111110111

FIG.4

Baud clock count = 0 — 80

Base clock count = 0 — 81

Increment
Base clock count — 82

Bit value selected by
REMD and Baud clock count? — 83

0 ⌐ 84

1   85

N | Base clock count = D? |

| Base clock count = D+1 ? | N

Y

Y

Generate baud
clock pulse — 86

Increment
Baud clock count — 87

— 88

N | Baud clock count = K ?

Y

FIG. 5

FIG. 6

Bit Interval

D+1 base clock cycles

D base clock cycles

time
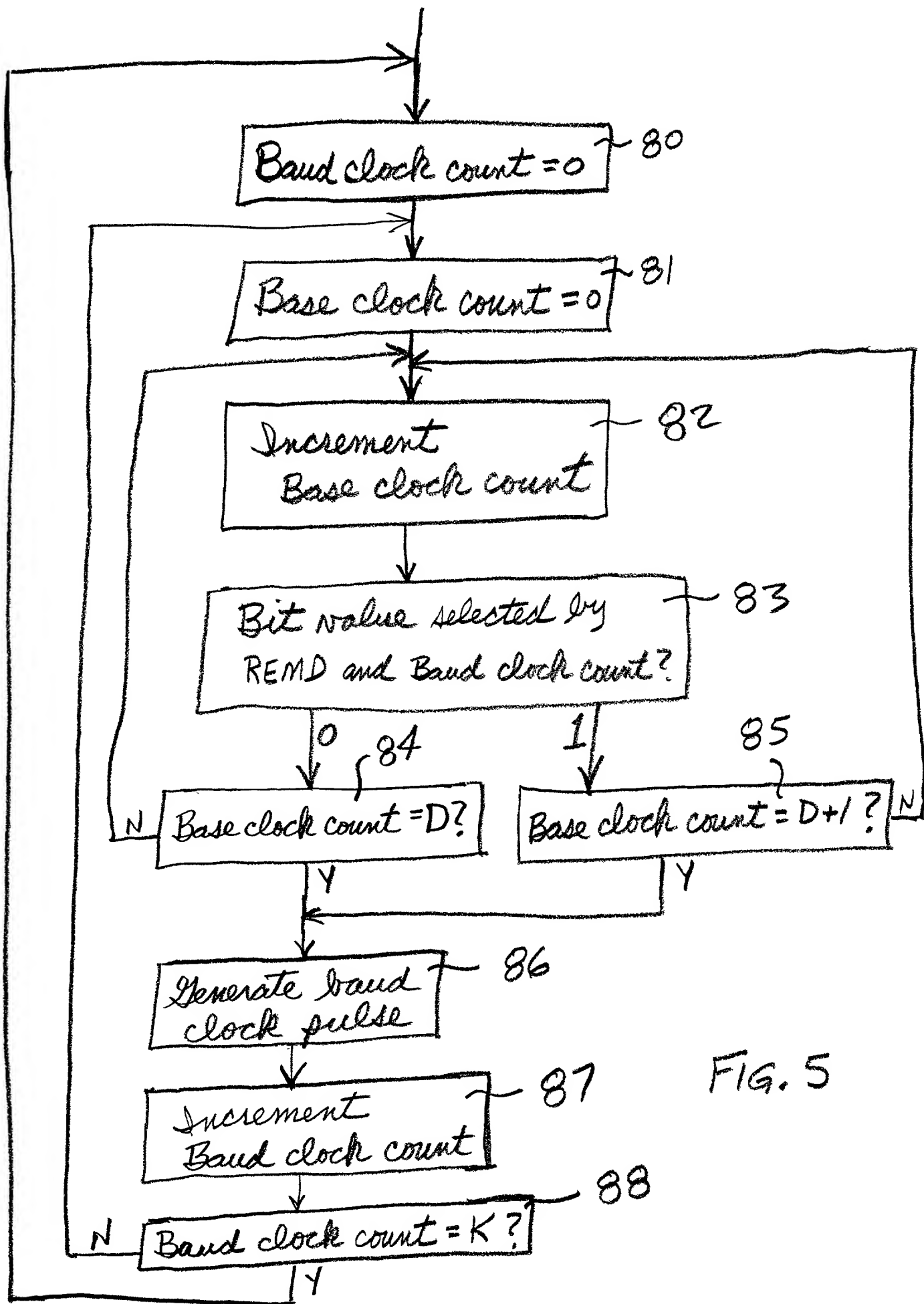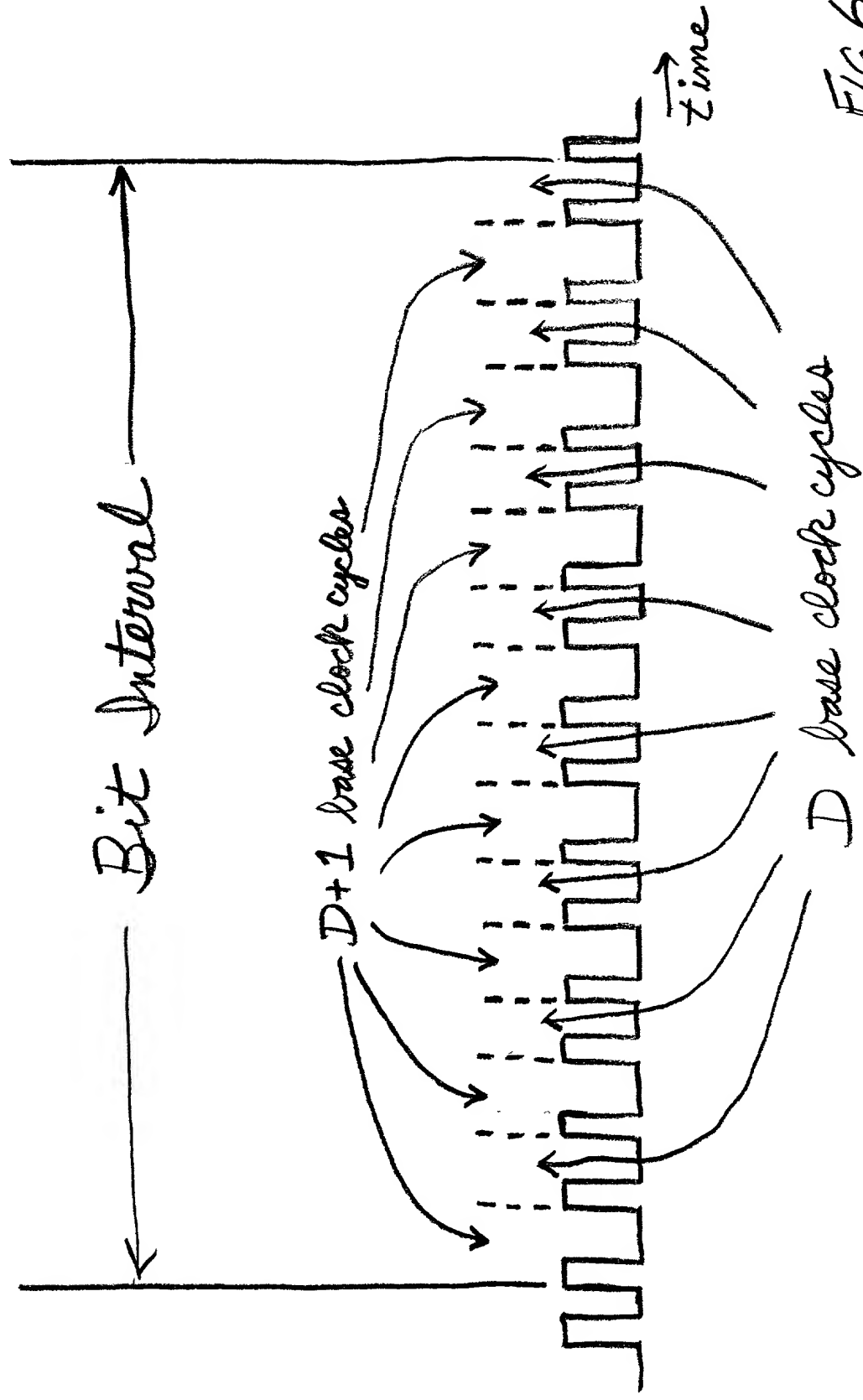
Baud Rate Ranges	D	REMD
Range 1	1	0
Range 2	1	1
Range 3	1	2
⋮	↓	⋮
Range K	1	K-1
Range K+1	2	0
Range K+2	2	1
Range K+3	2	2
⋮	↓	⋮
Range 2K	2	K-1
Range 2K+1	3	0
Range 2K+2	3	1
Range 2K+3	3	2
⋮	⋮	⋮

FIG. 8

data
processing
cktry   65

67   UART   61

69   FIG. 9

EXTERNAL
DEVICE(S)   63

71   New Baud   N
      Rate Desired?

            Y

73   Get D and
      REMD

      Use D and REMD   75
      to produce baud
      clock from base clock

                      FIG. 10

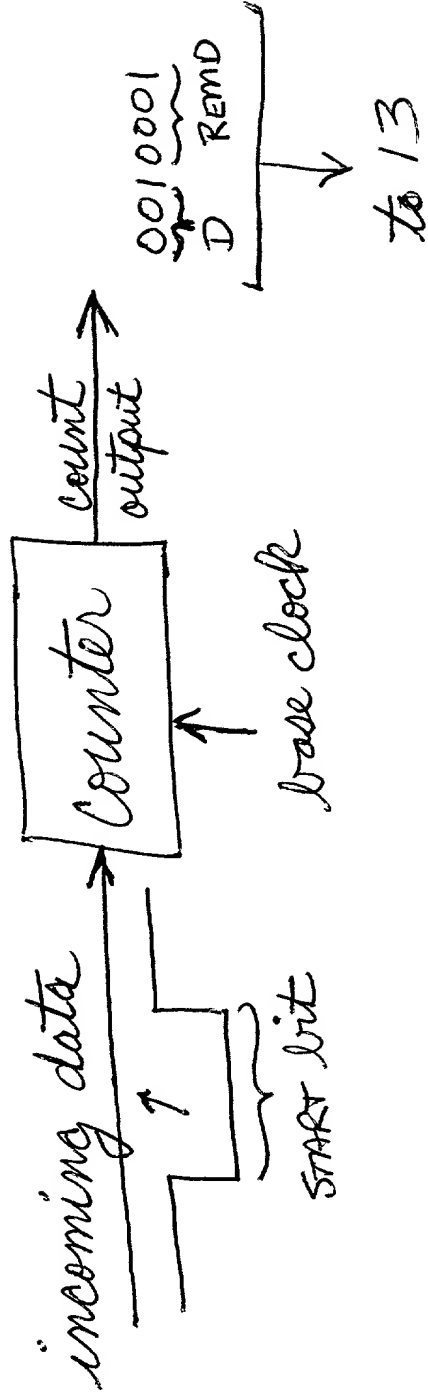incoming data
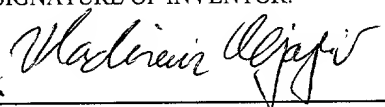
START bit

Counter

base clock

count
output

0010001
D   RemD

to 13
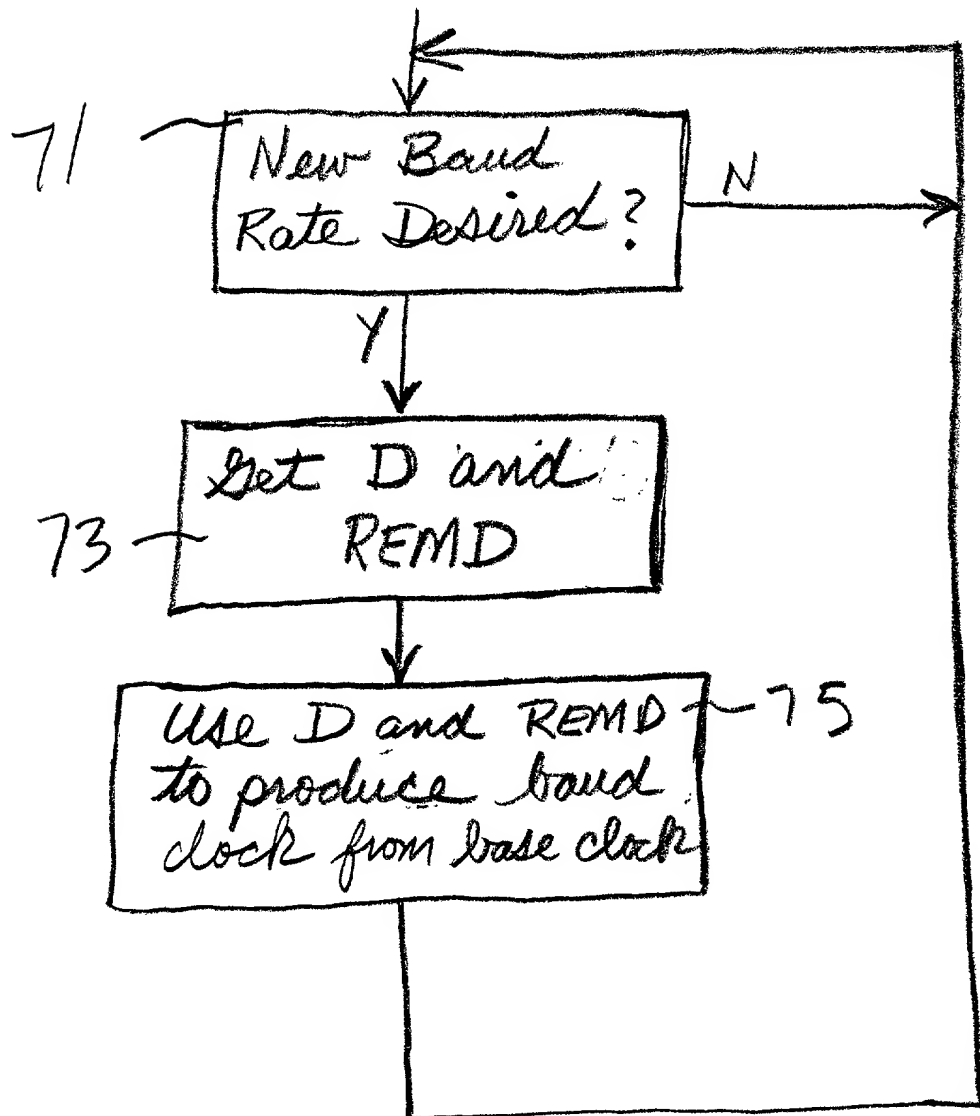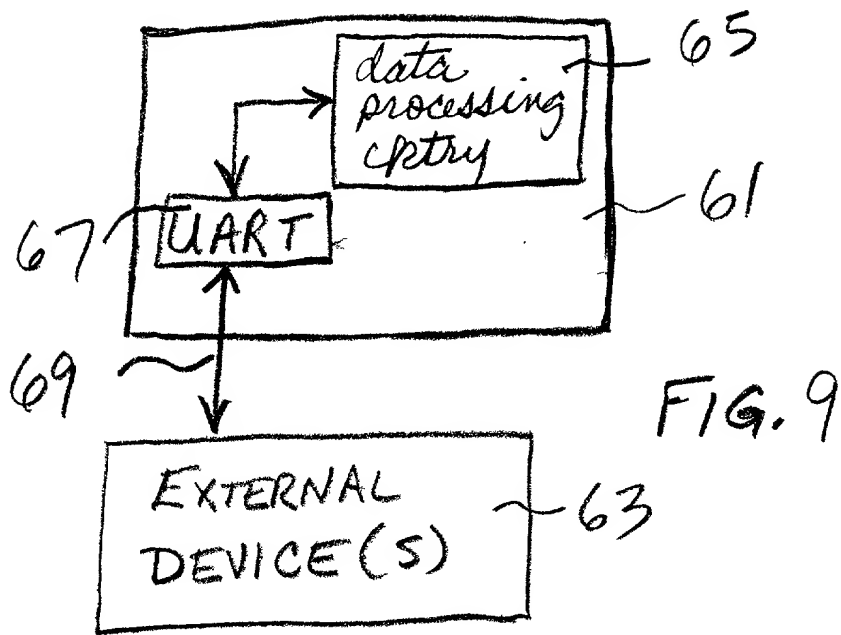
FIG. 11
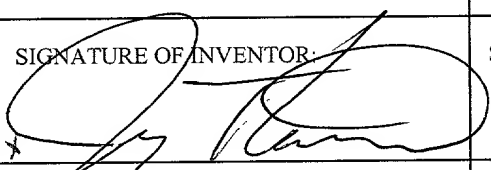
APPLICATION FOR UNITED STATES PATENT

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, section 1.56(a);

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION: **HIGH-SPEED, HIGH GRANULARITY BAUD CLOCK GENERATION**

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

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DATE: X 8/8/2000	DATE: X 8/8/2000	DATE: